Jaehyun Lim

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Education

Carnegie Mellon University Pittsburgh, PA

BS in Electrical and Computer Engineering with University Honors, 3.81 QPA *Aug. 2022 – Dec 2026*

- **Extracurricular Activities**: Board member and volunteer at ECE Outreach (electrical and computer engineering education outreach in Pittsburgh community), D Flat Singers Choir singer
- **Selected Coursework**: Modern Computer Architecture, Data Center Computing, Logic Design and Verification, Computer Networks, Introduction to Embedded Systems, Computer Systems and the Hardware-Software Interface

Technical Skills

Languages and tools: SystemVerilog, C++, C, Python, MLIR, LLVM, Git, VCS, Quartus, Vivado, Design Compiler

Experience

Undergraduate Research Assistant Dec. 2024 – Present

Abstract Lab @ CMU *Pittsburgh, PA*

- Co-developed a research project adding load-store queues to a dataflow architecture for out-of-order memory speculation, removing conservative memory-ordering constraints (paper submitted to ASPLOS 2027); implemented compiler support for hyperblock formation with MLIR and built a benchmarking suite across 6 workloads, achieving up to 19.9x speedup.
- Currently working on a compiler/PL project extending the capabilities of the Ripple Language (PLDI 2025) by adding automatic compilation to a new Ripple IR from C that makes programs map naturally to dataflow hardware.

Hardware Logic Intern June 2024 – Aug. 2024

Rebellions *Seongnam, South Korea*

- Designed a pipe-lined SECDED memory ECC system to meet 1.6 GHz target, making it parameterizable for any number of bit-widths in SystemVerilog, complete with random constrained testing.
- Programmed a Python script that runs a genetic algorithm design space exploration to optimize the parity-check matrix in terms of logic depth, power, size, and SDC rate with self-verifying ability using VCS and testbench.
- Realized up to 65% reduction in number of logic gate toggles, and 50% reduction with respect to SDC rate.

Teaching Assistant Spring 2024 – Spring 2025

Carnegie Mellon University, 18-240 Structure and Design of Digital Systems *Pittsburgh, PA*

- Led recitations, office hours, and lab sessions to teach concepts that include: combinational logic, clock timing, sequential logic design, RTL design, computer architecture, assembly and SystemVerilog.

Projects

Sniff Pittsburgh (Senior Capstone) | *Python, C, LoRaWAN, Flask, HTML, CSS, Docker* Dec 2025

- Created a mobile, low cost air quality monitoring solution to be mounted on POGOH bikeshare bikes with the goal of filling in gaps in existing air quality maps.
- Engineered the LoRaWAN, cellular, and HTTP communications stack of the system, creating a pathway for air quality data to be uploaded to our website.
- Designed and implemented sniffpittsburgh.com, a real time map of bicycle-collected air quality data across Pittsburgh.
- David Tuma Undergraduate Project Award – First Runner Up

MLIR Compiler | *C++, MLIR, Git* June 2025

- Created a compiler for a toy scripting language that emits MLIR with C++ lexer and parser and MLIR + LLVM backend.

RISC-V Processor | *SystemVerilog, Git* May 2025

- Created a pipelined RV32I core with cache prefetching, branch prediction, and data-forwarding.

Real-Time Operating System | *C, STM32, Fusion360, PCB fabrication, Git* Dec 2024

- Programmed an RTOS with RMS scheduling for up to 15 threads with context-switching, deadlines, and mutexes.

ATC on a Chip (Tapeout) | *SystemVerilog, cocoTB, Verilator, Yosys, OpenLane, Git* May 2024

- Used completely open source ASIC tool-chain to tape out a chip using Skywater's 130nm process. Implements a just-for-fun air traffic control system that manages a small-scale airport with two runways, managing communication with UART and FIFO queues.